Remarks/Arguments

Status of the Claims

- Claims 1-11 are pending in the Application after entry of this amendment.
- Claims 1-11 are rejected by Examiner.
- Claims 1, 2, 5, 6, 8 and 10 are amended by the present Amendment, claim 1 being amended by adding features of claim 2, as clearly illustrated by Figures 6-10 and 12-16; claim 1 being further amended for clarification by adding that the row address means comprise separate row address means for each of the block of rows, as described in Applicants' Specification at page 5, lines 29-31.

35 U.S.C. §112, ¶

Claims 5, 6 and 8 have been amended according to Examiner's suggestions so as to overcome the objections related to insufficient antecedent basis. Objected limitations of claim 2 have been cancelled from claim 2 and added in claim 1 with amendments suggested by the Examiner. Claim 10 is amended by adding that the switching means comprises a seventh diode (see figure 16 and the corresponding part of the Specification, i.e. on page 10, lines 30-36). The diode comprised in the switching means does not correspond to the second diode (referenced as D3 on figure 16), as the second diode (D3) is comprised in the sustain means (as claimed in claim 7). Claim 10 corresponds to an embodiment of applicant's invention wherein the switch (I10, I10') is replaced by a diode (D10, D10') in the switching means. This diode has been identified as a seventh diode in claim 10 for clarity reason, the seventh diode being oriented so as to not allow a current to flow in the direction of the first connection line (I1, I1'), as clearly described on page 10, lines 34-36 (for isolating the first connection line from the sustain means).

Applicant respectfully requests reconsideration of the 35 U.S.C. §112 rejection of pending Claims 2, 5, 6, 8 and 10 based on the remarks above.

35 U.S.C. §102 and 35 U.S.C. §103

Claims 1 and 11 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Awamoto (US 6369514 B2). Claims 1 and 11 have been amended to recite more clearly patentably distinguishable features.

Applicants' invention as recited in amended Claim 1 is a device for driving a plasma display panel having a plurality of cells arranged in rows and columns, the rows of cells being distributed in a plurality of blocks of lines (for example B1 or B2 of Figure 10), said device comprising row address means for selectively addressing the display cell rows within the blocks and creating, where required, in cooperation with means for selectively applying data voltages to the display columns, an electrical discharge inside the cell disposed at the intersection of the row and column selected during an address phase, and sustain means for sustaining the electrical discharges inside said cell during a sustain phase immediately following the address phase, wherein said row address means comprise separate row address means for each of the block of rows (for example B1, B2) for addressing successively the blocks of rows by applying a first voltage (for example Vbw1) to the cells of the selected block (for example B1) and a second voltage (for example Vbw2) to the cells of the other blocks (for example B2), said second voltage (for example Vbw2) being greater than the first voltage (for example Vbw1), said separate row address means comprising: at least one row driver circuit (for example 11) connected between first and second connection lines (for example L1 and L2) and designed to apply, during an address phase specific to said block of rows (for example B1), a potential of one of said first and second connection lines (for example L1) to a plurality of rows of the block; a capacitor (for example C1), a first terminal of which being coupled to the first connection line (for example L1) via a first switch (for example I1) and a second terminal of which being coupled to the second connection line (for example L2); a second switch (for example I2) for selectively applying an address voltage (for example Vw) to the second connection line (for example L2) during the address phase; a first diode (for example D1) connected to the common point of the first switch (for example I1) and of the capacitor (for example C1) for supplying the first voltage (for example Vbw1) to the capacitor (for example C1) during the address phase.

In contrast to the recitations in Amended Claim 1, Awamoto does not disclose or suggest that the separate row address means comprise a capacitor, a first terminal of which being connected to the first connection line via a first switch and a second terminal of which being connected to the second connection line; and a first diode connected to the common point of the first switch and of the capacitor for supplying the first voltage to the capacitor during the address phase.

As acknowledged by the Examiner, Awamoto does not teach any capacitor for connecting the cathode of a first diode to the second connection line (see Office Action on page 7), i.e. Awamoto does not teach that a capacitor is connected between the first connection line via a first switch and the second connection line. The Examiner asserts that it is well known in the art to include a capacitor for connecting a cathode of a diode to a connection line. Applicants respectfully disagree. First, no prior art is cited disclosing such a feature. Second, as explained in Applicants' Specification on page 7, lines 17-20, such a capacitor C1 being connected to the terminals of the driver circuits guarantees in combination with the diode D1 that a correct supply voltage is maintained between the terminals of the driver circuits. Moreover, C1 provides a current path for bidirectional current coming from the panel (see for example applicants' Figures 12 and 13). Without such a capacitor C1, bidirectional current flowing from the panel would not be able to flow through the address means, which could generate overvoltages across the driver(s). Diode D1 enables passive regulation of the voltage at the terminals of C1. By contrast to the arrangement as claimed in claim 1 comprising the capacitor C1, the arrangement of Awamoto (see for example Fig. 8) comprises diodes connected respectively in series with the switches Q51 and Q61, such diodes not allowing the current coming from the panel to flow bidirectionally in the address means, such that undesirable overvoltages can be created across the drivers. Thus, the arrangement of Awamoto is radically different from Applicants' arrangement as recited in claim 1 because the arrangement of Awamoto is able neither to avoid overvoltages nor to maintain a correct voltage between the terminals of the driver circuits.

Therefore, Awamoto does not teach or suggest the inventive combination recited in Amended Claim 1 including the separate row address means comprising a capacitor, a first terminal of which being coupled to the first connection line via a first switch and a second terminal of which being coupled to the second connection line; a second switch for selectively applying an address voltage to the second connection line during the address phase; and a first diode connected to the common point of the first switch and of the capacitor for supplying the first voltage to the capacitor during the address phase.

Applicant respectfully submits that pending independent claim 1 is unobvious and inventive over Awamoto because some of the elements of the pending claim 1 are not found in Awamoto. Claims 2-11 are also not anticipated because they depend from non-anticipated independent claim 1. Having fully addressed the Examiner's rejections it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion

that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at (609) 734-6812, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,
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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being transmitted via facsimile to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 2313-1450 on July 25 2011, at facsimile number (571) 273-8300.

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